

## CLAIMS

What is claimed is:

1. A receiver for acquiring composite pseudo-noise (PN) encoded signals, the receiver comprising:

a receiver demodulator;

a first receiver clock generator;

at least three first receiver pseudo-noise (PN) component code generators coupled to the first receiver clock generator;

a receiver logic combiner coupled to the at least three first receiver PN component code generators, the receiver logic combiner adapted to generate a local epoch symmetrical composite PN code, wherein the local epoch symmetrical composite PN code comprises at least three PN component codes, wherein the at least three PN component codes are relatively prime.

2. A receiver as in claim 1 wherein the at least three first receiver pseudo-noise (PN) component code generators comprise four first receiver PN component code generators.

3. A receiver as in claim 1 wherein the receiver demodulator is adapted to generate a normalized epoch autonomous phase (NEAP), wherein the NEAP comprises the form:

$$(N_{xy} \times L_x \times L_y) \text{MOD}(L_x \times L_z) = L_x$$

where  $N_{xy}$  = integer number of  $L_x L_y$  epochs of interest, and  
 $L_{(PN...PN...)} =$  epoch length of PN component codes.

4. A receiver as in claim 3 wherein the receiver demodulator is adapted to generate a normalized epoch autonomous phase (NEAP), wherein the NEAP comprises the form:

$$(N_{MXY} \times L_x \times L_y) \text{ MOD } (L_x \times L_z) = L_x M$$

where  $N_{xy}$  = integer variable number of  $L_x L_y$  epochs of interest,  $M$ =integer variable number of  $L_x$  epochs, and  
 $L_{(PN...PN...)} =$  epoch length of PN component codes.

5. A receiver as in claim 3 wherein the receiver demodulator is adapted to adjust a local epoch symmetrical composite PN code phase according to the NEAP.

6. A receiver as in claim 1 wherein the receiver logic combiner comprises a MAND logic combiner.

7. A receiver as in claim 1 wherein the receiver logic combiner comprises a MAJ logic combiner.

8. A method for determining Psuedo-Noise (PN) composite phase, the method comprising:

providing at least three PN component codes, wherein the at least three PN component codes are relatively prime;

partially correlating a received PN composite encoded signal with a first minor epoch;

searching for phase alignment of the received PN composite encoded signal with a second minor epoch; and

correlating the received PN composite encoded signal with a receiver PN composite code phase when the first minor epoch and the second minor epoch are separated by a predetermined phase.

9. A method as in claim 8 wherein providing the plurality of relatively prime PN component codes further comprises:

providing at least three relatively prime PN component codes, wherein the at least three relatively prime PN component comprise at least:

a first minor epoch;

a second minor epoch; and

determining a normalized epoch autonomous phase associated with the first minor epoch and the second minor epoch.

10. A method as in claim 8 wherein generating the PN composite code from the PN component codes further comprises logically combining the plurality of PN codes according to MAND logic

11. A method as in claim 8 wherein generating the PN composite code from the PN component codes further comprises logically combining the plurality of PN codes according to MAJ logic.

12. A method as in claim 9 wherein correlating the received PN composite encoded signal with the receiver PN composite code phase further comprises:

searching for the normalized autonomous epoch phase substantially in steps of the first minor epoch;

finding the normalized autonomous epoch phase; and

determining composite phase resulting from finding the normalized autonomous epoch phase.

13. An integrated circuit (IC), wherein the IC comprises:

at least three receiver pseudo-noise (PN) component code generators  $PN_x$ ,  $PN_y$ ,  $PN_z$ , wherein each PN component code generator is adapted to generate relatively prime PN component codes when compared with each of the other PN component code generators; and

a Normalized Epoch Autonomous Phase Number (NEAP) generator for generating at least one NEAP.

14. An IC as in claim 13 wherein the IC comprises an Application Specific IC (ASIC).

15. An IC as in claim 13 wherein the IC comprises a field programmable gate array (FPGA).

16. An IC as in claim 13 further wherein the NEAP generator comprises a NEAP look-up-table.

17. An IC as in claim 13 wherein the IC further comprises an X-epoch counter.

18. An IC as in claim 17 wherein the X-epoch counter further comprises:

at least one XY-epoch latched counter; and

at least one XZ-epoch latched counter.

19. An IC as in claim 13 wherein the IC further comprises:

at least one sampling clock count input;

at least one time-since-initialization (TSI) generator;

at least one TSI\_latched sampling clock counter coupled to the at least one TSI generator and the at least one sampling clock count input; and

at least one XY\_latched sampling clock counter coupled to the at least one sampling clock count input.

20. An IC as in claim 13 wherein the IC comprises an Application Specific IC (ASIC).

21. An IC as in claim 13 wherein the IC comprises a field programmable gate array (FPGA).

22. A program storage device readable by a machine, tangibly embodying a program of instructions executable

by the machine to perform method steps for determining Psuedo-Noise (PN) composite phase, the method comprising:

providing at least three PN component codes, wherein the at least three PN component codes are relatively prime;

partially correlating a received PN composite encoded signal with a first minor epoch;

searching for phase alignment of the received PN composite encoded signal with a second minor epoch; and

correlating the received PN composite encoded signal with a receiver PN composite code phase when the first minor epoch and the second minor epoch are separated by a predetermined phase.

23. A program storage device as in claim 22 wherein the program of instructions comprise at least one Very High Speed Integrated Circuit (VHSIC) Hardware Description (VHDL) Language file.